Hall Ticket Number:

Code No.: 21513 S

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. II Year (I.T.) I-Semester Supplementary Examinations, May/June-2017

Digital Electronics and Logic Design

Time: 3 hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 X 2=20 Marks)

1. Realize the following Boolean expression using only NAND gate and only NOR gate.
   $g = ab'c + a'bc + abc$
2. Show the following expression using Karnaugh map method in SOP form.
   $F = xy + x'(xy + yz) + y(y + (xz)')$
3. Distinguish between CPLD and FPGA devices.
4. Explain the concept encoding and decoding.
5. Describe propagation delay and setup time of a D flip flop.
6. Explain the race-around problem in JK-FF.
7. Determine f_{max} of a mod -16 binary counter.
8. Develop a behavioral VHDL model for positive edge triggered D flip flop.
9. Define about cycles in asynchronous sequential circuits.
10. Describe essential hazard in asynchronous sequential circuits.

Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) Design an even parity generator for an 8-bit of data.
    b) Design Carry look ahead adder with suitable equations and diagrams.
12. a) Develop a structural VHDL model for 2-bit magnitude comparator.
    b) Design the difference and carry function of a full subtractor using PLA and PAL devices.
13. a) Distinguish between the level triggered and an edge triggered T-FF with the help of timing diagrams.
    b) Design a decade counter using flip flops and gates.
14. a) Explain the FSM as an arbiter circuit.
    b) Draw the state diagram to detect the sequence 101 from input sequence, Design sequential circuit using JK flip flops for the same.
15. a) Draw ASM chart for the controller of 4×4 a sequential shift and add multiplier.
    b) Describe design steps for asynchronous sequential circuits.
16. a) Design a circuit that will accept 8-bit signed numbers as input and generates 2's complement of it, as output.
    b) Explain the functionality of Logic element and routing matrix in a CPLD.
17. Write short notes on any ***two*** of the following:
    a) Distinguish between Mealy and Moore model.
    b) Explain Static Hazards with examples.
    c) Discuss about transition table and flow table.